ABSTRACT OF THE DISCLOSURE

Provided is a circuit that has a simple circuit configuration and can detect zero values in a 1-bit digital signal irrespective of a recording medium such as SACD. DSD data forming the 1-bit digital signal are successively sent to a shift register (1) whose number of stages corresponds to the number of bits of an idle pattern such as "101010101" which appears when assuming a zero value. For example, the shift register (1) is an 8-bit shift register. An adder (2) sums up the values at each stages of the shift register (1). A zero decision circuit (4) produces an output indicating decision of zero if the sum value is half of the number of bits. A counter (5) keeps counting while the output indicating zero decision is being delivered. If the count value of the counter exceeds a given value, the counter produces an output indicating detection of a zero value. In consequence, zero values in a 1-bit digital signal can be detected with a simple circuit configuration, regardless of the idle pattern that varies among different recording media such as SACDs.